

Digital FET, N-Channel

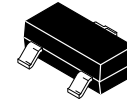
FDV303N

General Description

These N-Channel enhancement mode field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process is tailored to minimize on-state resistance at low gate drive conditions. This device is designed especially for application in battery circuits using either one lithium or three cadmium or NMH cells. It can be used as an inverter or for high-efficiency miniature discrete DC/DC conversion in compact portable electronic devices like cellular phones and pagers. This device has excellent on-state resistance even at gate drive voltages as low as 2.5 V.

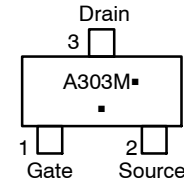
Features

- 25 V, 0.68 A Continuous, 2 A Peak
 - ♦ $R_{DS(ON)} = 0.45 \Omega @ V_{GS} = 4.5 V$
 - ♦ $R_{DS(ON)} = 0.6 \Omega @ V_{GS} = 2.7 V$
- Very Low Level Gate Drive Requirements Allowing Direct Operation in 3 V Circuits, $V_{GS(th)} < 1 V$
- Gate-Source Zener for ESD Ruggedness, > 6 kV Human Body Model
- Compact Industry Standard SOT-23 Surface Mount Package
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant



SOT-23 (TO-236)
CASE 318-08
STYLE 21

MARKING DIAGRAM



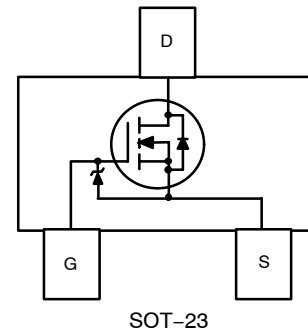
A or blank = One/two character Location Code
 303 = Specific Device Code
 M = Date Code
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

* Location code can be blank or with characters indicating manufacturing location

* Date Code orientation and overbar may vary depending upon manufacturing location.

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDV303N

MOSFET MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDV303N	Units
V_{DSS}	Drain–Source Voltage, Power Supply Voltage	25	V
V_{GSS}	Gate–Source Voltage, V_{IN}	8	V
I_{D}	Drain/Output Current – Continuous – Pulsed	0.68 2	A
P_{D}	Maximum Power Dissipation	0.35	W
$T_{\text{J}}, T_{\text{STG}}$	Operating and Storage Temperature Range	–55 to 150	$^\circ\text{C}$
ESD	Electrostatic Discharge Rating MIL–STD–883D Human Body Model (100 pF / 1500 Ω)	6.0	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Units
$R_{\theta\text{JA}}$	Thermal Resistance, Junction–to–Ambient	357	$^\circ\text{C/W}$

ORDERING INFORMATION

Device	Package	Shipping [†]
FDV303N	SOT–23 Case 318–08	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

FDV303N

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
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OFF CHARACTERISTICS

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		26		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$T_J = 55^\circ\text{C}$			10	μA
I_{GSS}	Gate – Body Leakage Current	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA

ON CHARACTERISTICS (Note 1)

$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		–2.6		mV/ $^\circ\text{C}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.65	0.8	1	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 0.5\text{ A}$		0.33	0.45	Ω
		$T_J = 125^\circ\text{C}$		0.52	0.8	
		$V_{GS} = 2.7\text{ V}, I_D = 0.2\text{ A}$		0.44	0.6	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 2.7\text{ V}, V_{DS} = 5\text{ V}$	0.5			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 0.5\text{ A}$		1.45		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		50		pF
C_{oss}	Output Capacitance			28		pF
C_{rss}	Reverse Transfer Capacitance			9		pF

SWITCHING CHARACTERISTICS (Note 1)

$t_{D(on)}$	Turn – On Delay Time	$V_{DD} = 6\text{ V}, I_D = 0.5\text{ A}, V_{GS} = 4.5\text{ V}, R_{GEN} = 50\text{ }\Omega$		3	6	ns
t_r	Turn – On Rise Time			8.5	18	ns
$t_{D(off)}$	Turn – Off Delay Time			17	30	ns
t_f	Turn – Off Fall Time			13	25	ns
Q_g	Total Gate Charge	$V_{DS} = 5\text{ V}, I_D = 0.5\text{ A}, V_{GS} = 4.5\text{ V}$		1.64	2.3	nC
Q_{gs}	Gate–Source Charge			0.38		nC
Q_{gd}	Gate–Drain Charge			0.45		nC

DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current				0.3	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.5 A (Note 1)		0.83	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%.

TYPICAL CHARACTERISTICS

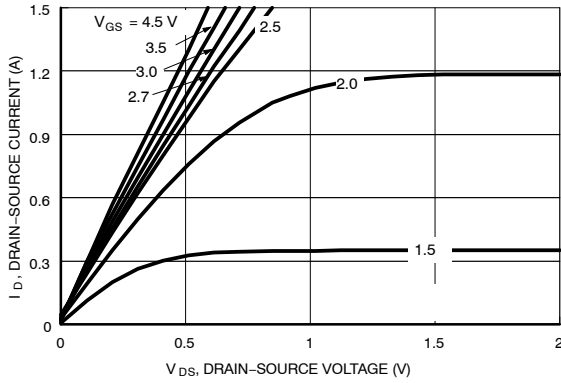


Figure 1. On-Region Characteristics

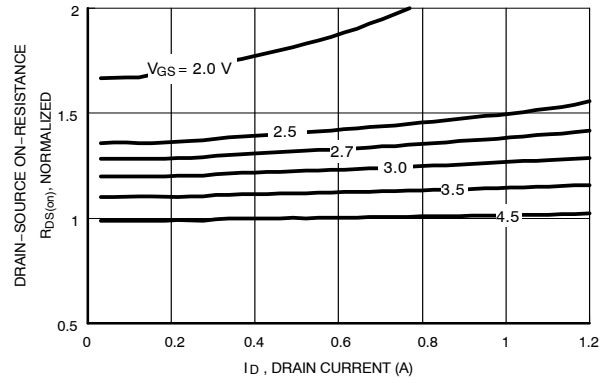


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

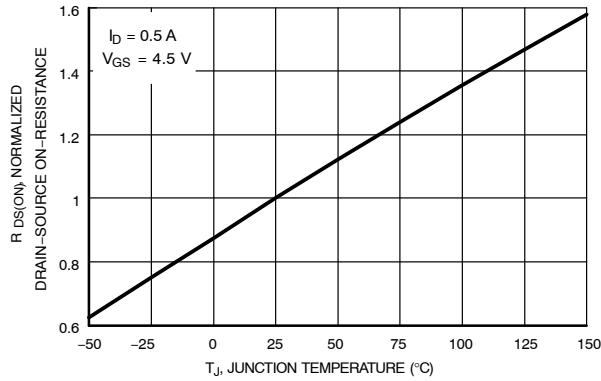


Figure 3. On-Resistance Variation with Temperature

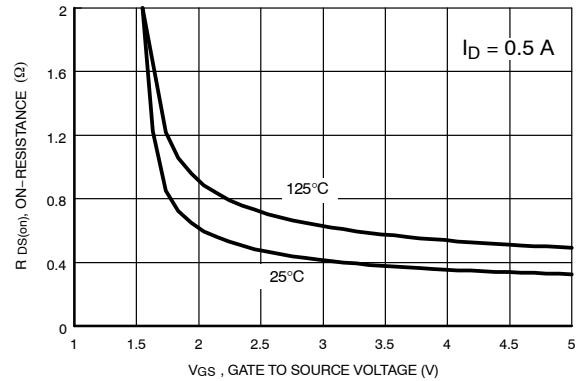


Figure 4. On Resistance Variation with Gate-To-Source Voltage

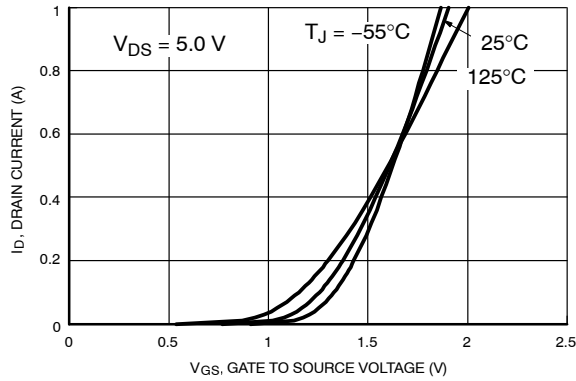


Figure 5. Transfer Characteristics

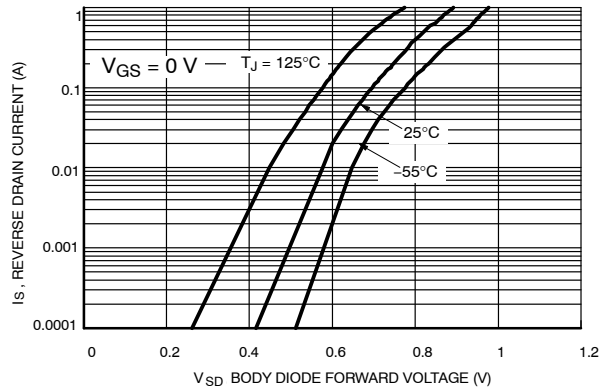


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ Unless Otherwise Noted (continued)

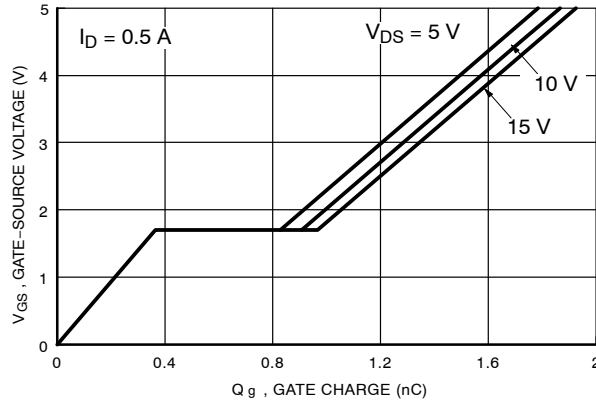


Figure 7. Gate Charge Characteristics

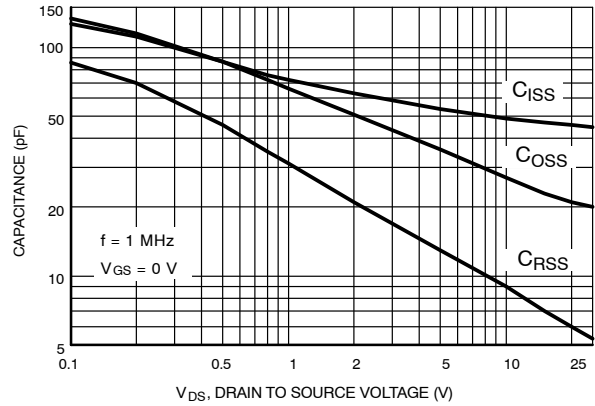


Figure 8. Capacitance Characteristics

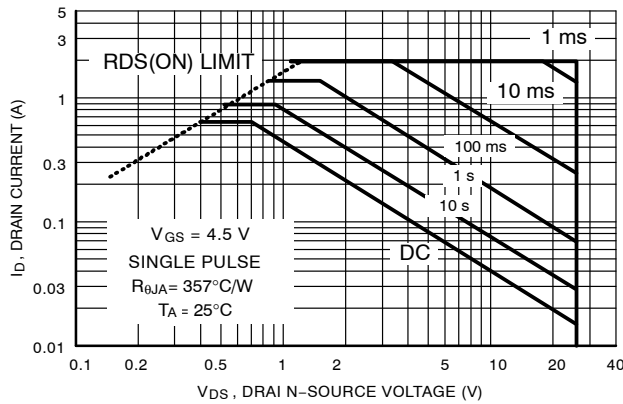


Figure 9. Maximum Safe Operating Area

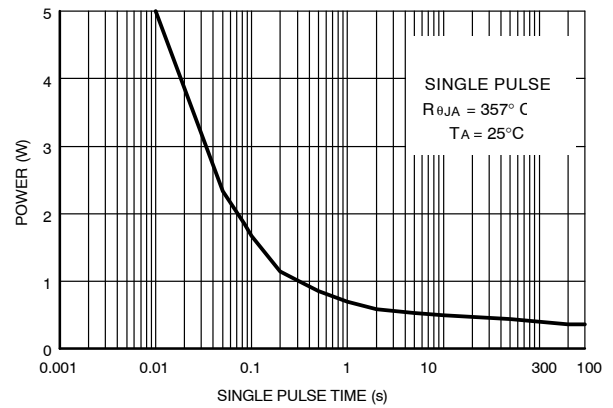


Figure 10. Single Pulse Maximum Power Dissipation

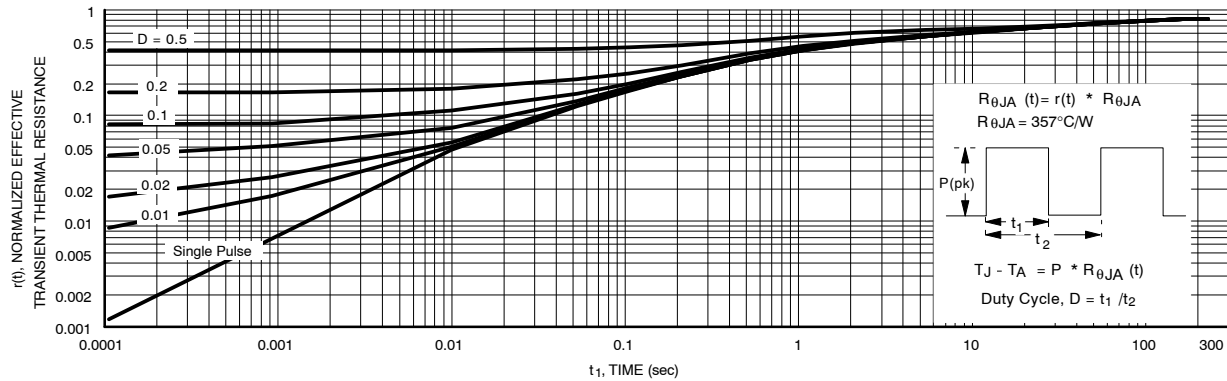


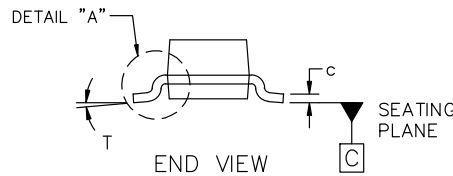
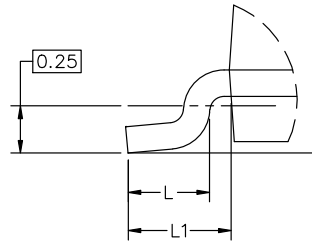
Figure 11. Transient Thermal Response Curve



SCALE 4:1

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CASE 318
ISSUE AU

DATE 14 AUG 2024

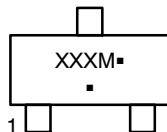


MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
HE	2.10	2.40	2.64
T	0°	---	10°

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

STYLES ON PAGE 2

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STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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